CY14E256L

256 Kbit (32K x 8) nvSRAM

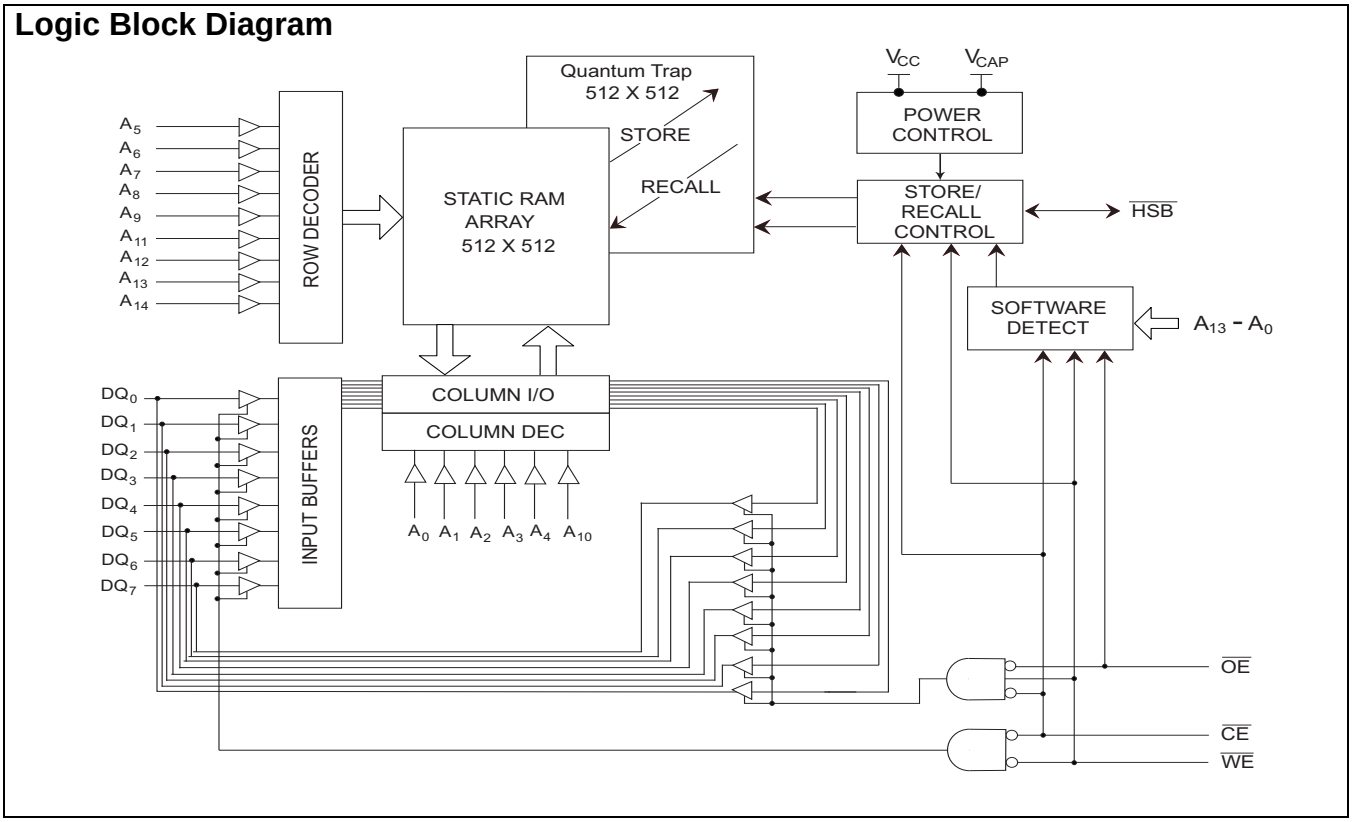
Features

- 25 ns, 35 ns, and 45 ns access times
- Pin compatible with STK14C88
- Hands off automatic STORE on power down with external 68 µF capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power down
- RECALL to SRAM initiated by software or power up
- Unlimited READ, WRITE, and RECALL cycles
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5V±10% operation
- Commercial and industrial temperature
- 32-pin SOIC and CDIP (300 mil) packages
- RoHS compliance

Functional Description

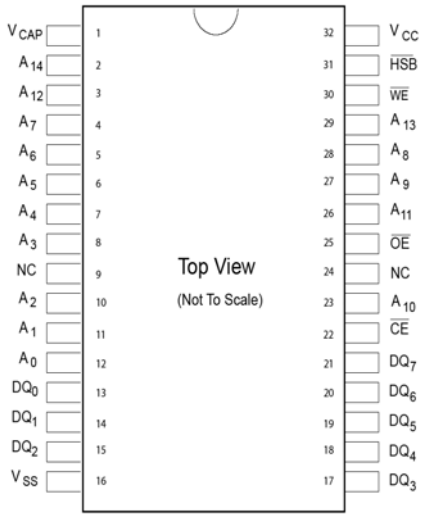
The Cypress CY14E256L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control. A hardware STORE is initiated with the $\overline{HSB}$ pin.

Logic Block Diagram



Pin Configurations

Figure 1. Pin Diagram: 32-Pin SOIC/DIP



Pin Definitions

Pin Name	Alt	IO Type	Description
A_0–A_{14}		Input	**Address Inputs.** Used to select one of the 32,768 bytes of the nvSRAM.
DQ_0-DQ_7		Input or Output	**Bidirectional Data IO Lines**. Used as input or output lines depending on operation.
$\overline{WE}$	$\overline{W}$	Input	**Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the IO pins is written to the specific address location.
$\overline{CE}$	$\overline{E}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	$\overline{G}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.
V_{SS}		Ground	**Ground for the Device**. The device is connected to ground of the system.
V_{CC}		Power Supply	**Power Supply Inputs to the Device**.
$\overline{HSB}$		Input or Output	**Hardware Store Busy (HSB)**. When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional).
V_{CAP}		Power Supply	**AutoStore Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

[+] Feedback

Device Operation

The CY14E256L nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The CY14E256L supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

SRAM Read

The CY14E256L performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins $A_{0–14}$ determines the 32,768 data bytes accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and HSB is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common IO pins $DQ_{0–7}$ are written into the memory if it has valid t_{SD}, before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. Keep $\overline{OE}$ HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14E256L stores data to nvSRAM using one of three storage operations:

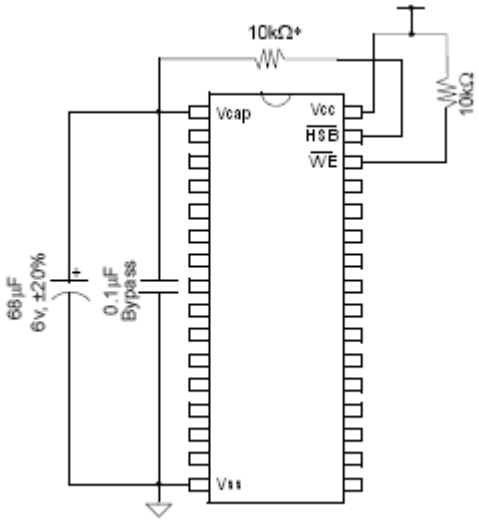
1. Hardware store activated by $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14E256L.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. A charge storage capacitor having a capacitor of between 68uF and 220uF (± 20%) rated at 6V should be provided. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up is placed on $\overline{WE}$ to hold it inactive during power up.

Figure 2. AutoStore Mode



In system power mode, both V_{CC} and V_{CAP} are connected to the +5V power supply without the 68 µF capacitor. In this mode, the AutoStore function of the CY14E256L operates on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10 ms STORE cycle.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored, unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. An optional pull-up resistor is shown connected to $\overline{HSB}$. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

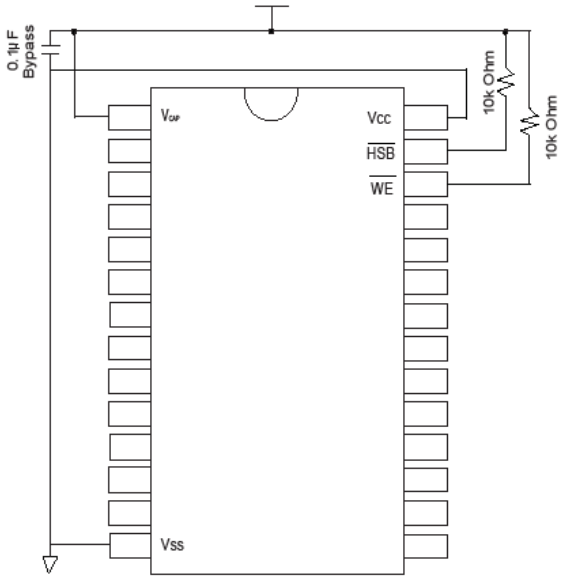
If the power supply drops faster than 20 us/volt before Vcc reaches V_{SWITCH}, then a 2.2 ohm resistor should be connected between V_{CC} and the system supply to avoid momentary excess of current between V_{CC} and V_{CAP}.

AutoStore Inhibit mode

If an automatic STORE on power loss is not required, then V_{CC} is tied to ground and + 5V is applied to V_{CAP} (Figure 3). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the CY14E256L is operated in this configuration, references to V_{CC} are changed to V_{CAP} throughout this data sheet. In this mode, STORE operations are triggered through software control or the HSB pin. To enable or disable Autostore using an I/O port pin see “” on page 5. It is not permissible to change between these three options” on the fly”.

[+] Feedback

Figure 3. AutoStore Inhibit Mode



Hardware STORE ($\overline{HSB}$) Operation

The CY14E256L provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin is used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the CY14E256L conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM takes place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to V_{CAP} if $\overline{HSB}$ is used as a driver.

SRAM READ and WRITE operations, that are in progress when $\overline{HSB}$ is driven LOW by any means, are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes LOW, the CY14E256L continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations take place. If a WRITE is in progress when $\overline{HSB}$ is pulled LOW, it allows a time, t_{DELAY} to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH.

During any STORE operation, regardless of how it is initiated, the CY14E256L continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the CY14E256L remains disabled until the $\overline{HSB}$ pin returns HIGH.

If $\overline{HSB}$ is not used, it is left unconnected.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC} < V_{RESET}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

If the CY14E256L is in a WRITE state at the end of power up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 Kohm resistor is connected either between $\overline{WE}$ and system V_{CC} or between $\overline{CE}$ and system V_{CC}.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14E256L software STORE cycle is initiated by executing sequential $\overline{CE}$ controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence is clocked with $\overline{CE}$ controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence. It is not necessary that $\overline{OE}$ is LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled READ operations is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared, and then the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

[+] Feedback

Data Protection

The CY14E256L protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14E256L is in a WRITE mode (both $\overline{CE}$ and $\overline{WE}$ are low) at power up after a RECALL or after a STORE, the WRITE is inhibited until a negative transition on $\overline{CE}$ or $\overline{WE}$ is detected. This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

The CY14E256L is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Hardware Protect

The CY14E256L offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low voltage conditions. When V_{CAP}<V_{SWITCH}, all externally initiated *STORE* operations and SRAM WRITEs are inhibited. AutoStore can be completely disabled by tying VCC to ground and applying + 5V to V_{CAP}. This is the AutoStore Inhibit mode; in this mode, *STORE*s are only initiated by explicit request using either the software sequence or the $\overline{HSB}$ pin.

Low Average Active Power

CMOS technology provides the CY14E256L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 4 shows the relationship between I_{CC} and READ or WRITE cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 5.5V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14E256L depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of READs to WRITEs
- CMOS versus TTL input levels
- The operating temperature
- The V_{CC} level
- IO loading

Figure 4. Current Versus Cycle Time (READ)

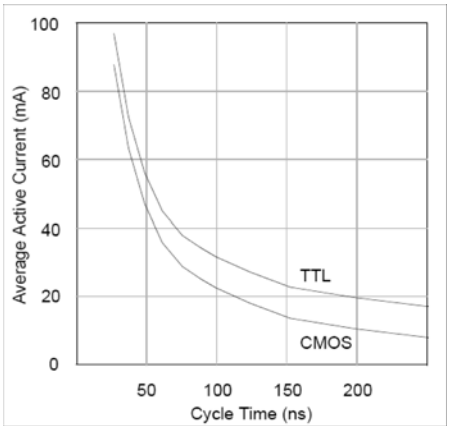
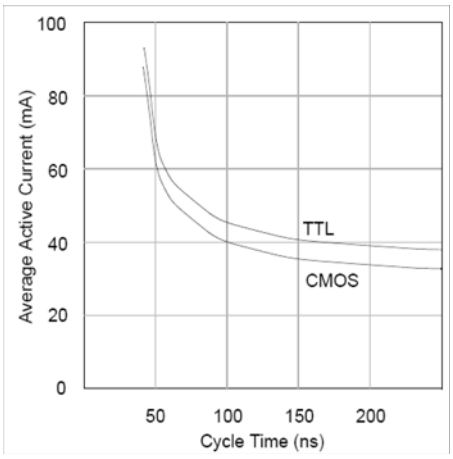


Figure 5. Current Versus Cycle Time (WRITE)



Preventing Store

The STORE function is disabled by holding $\overline{HSB}$ high with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2V, because it has to overpower the internal pull down device. This device drives $\overline{HSB}$ LOW for 20 µs at the onset of a STORE. When the CY14E256L is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68 µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the CY14E256L attempts to pull $\overline{HSB}$ LOW. If $\overline{HSB}$ does not actually get below V_{IL}, the part stops trying to pull $\overline{HSB}$ LOW and abort the STORE attempt.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers that want to use a larger V_{CAP} value to make sure there is extra store charge should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Table 1. Hardware Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{HSB}$	A13–A0	Mode	IO	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active[1]
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High Z	I_{CC2}[2]
L	H	H	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[1, 3, 4, 5] I_{CC2}
L	H	H	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[1, 3, 4, 5]

Notes
1. I/O state assumes $\overline{OE} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{OE}$.
2. HSB STORE operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the STORE (if any) completes, the part goes into standby mode, inhibiting all operations until HSB rises.
3. $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH for output behavior.
4. The six consecutive addresses must be in the order listed. $\overline{WE}$ must be high during all six consecutive $\overline{CE}$ controlled cycles to enable a nonvolatile cycle.
5. While there are 15 addresses on the CY14E256L, only the lower 14 are used to control software modes.

[+] Feedback

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 7.0V

Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC} + 0.5V

Input Voltage.....–0.5V to Vcc + 0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Lead Soldering Temperature (3 Seconds) ..... +260°C

DC output Current (1 output at a time, 1s duration) .... 15 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	4.5V to 5.5V
Industrial	-40°C to +85°C	4.5V to 5.5V

DC Electrical Characteristics

Over the operating range (V_{CC} = 4.5V to 5.5V) [6]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		97 80 70	mA mA
			Industrial		100 85 70	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{RC}= 200 ns, 5V, 25°C Typical	$\overline{WE} \geq (V_{CC} – 0.2V)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			2	mA
I_{SB} [7]	V_{CC} Standby Current	$\overline{CE} \geq (V_{CC} – 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} – 0.2V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			1.5	mA
I_{SB1} [7]	V_{CC} Standby Current (Standby, Cycling TTL Input Levels)	t_{RC} = 25 ns, $\overline{CE} \geq V_{IH}$ t_{RC} = 35 ns, $\overline{CE} \geq V_{IH}$ t_{RC} = 45 ns, $\overline{CE} \geq V_{IH}$	Commercial		30 25 22	mA mA mA
			Industrial		31 26 23	mA mA mA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		-1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		-5	+5	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –4 mA		2.4		V

Notes

6. V_{CC} reference levels throughout this data sheet refer to V_{CC} if that is where the power supply connection is made, or V_{CAP} if V_{CC} is connected to ground.
7. $\overline{CE} \geq V_{IH}$ does not produce standby current levels until any nonvolatile cycle in progress has timed out.

[+] Feedback

DC Electrical Characteristics

Over the operating range (continued)(V_{CC} = 4.5V to 5.5V) [6]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OL}	Output LOW Voltage	I_{OUT} = 8 mA		0.4	V
V_{BL}	Logic '0' Voltage on $\overline{HSB}$ Output	I_{OUT} = 3 mA		0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and Vss, 6V rated. 68 µF ±20% nom.	54	260	uF

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	100	Years
NV_C	Nonvolatile STORE Operations	1,000	K

Capacitance

In the following table, the capacitance parameters are listed.[8]

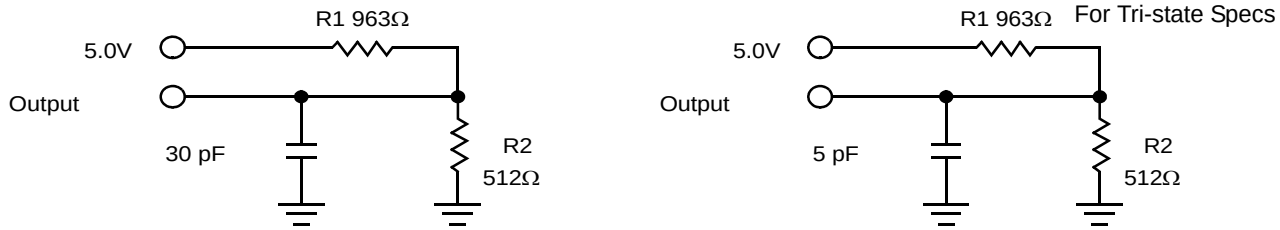
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[8]

Parameter	Description	Test Conditions	32-SOIC	32-CDIP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	35.45	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		13.26	TBD	°C/W

Figure 6. AC Test Loads



AC Test Conditions

Input Pulse Levels ..... 0V to 3V
Input Rise and Fall Times (10% - 90%)..... ≤5 ns
Input and Output Timing Reference Levels..... 1.5V

Note
8. These parameters are guaranteed by design and are not tested.

[+] Feedback

AC Switching Characteristics

SRAM Read Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{ACE}	t_{ELQV}	Chip Enable Access Time		25		35		45	ns
t_{RC} [9]	t_{AVAV}, t_{ELEH}	Read Cycle Time	25		35		45		ns
t_{AA} [10]	t_{AVQV}	Address Access Time		25		35		45	ns
t_{DOE}	t_{GLQV}	Output Enable to Data Valid		10		15		20	ns
t_{OHA} [10]	t_{AXQX}	Output Hold After Address Change	5		5		5		ns
t_{LZCE} [11]	t_{ELQX}	Chip Enable to Output Active	5		5		5		ns
t_{HZCE} [11]	t_{EHQZ}	Chip Disable to Output Inactive		10		13		15	ns
t_{LZOE} [11]	t_{GLQX}	Output Enable to Output Active	0		0		0		ns
t_{HZOE} [11]	t_{GHQZ}	Output Disable to Output Inactive		10		13		15	ns
t_{PU} [8]	t_{ELICCH}	Chip Enable to Power Active	0		0		0		ns
t_{PD} [8]	t_{EHICCL}	Chip Disable to Power Standby		25		35		45	ns

Switching Waveforms

Figure 7. SRAM Read Cycle 1: Address Controlled [9, 10]

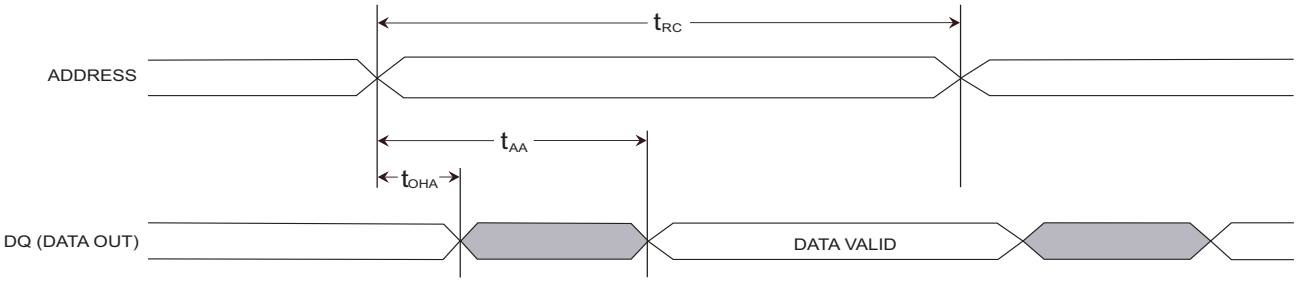
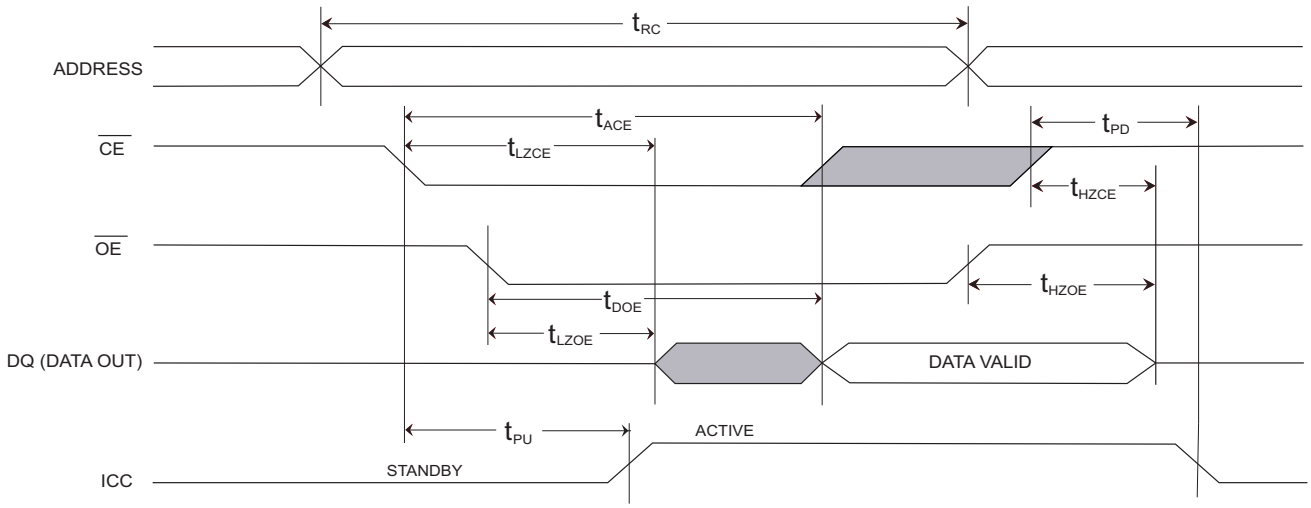


Figure 8. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled [9]



Notes
9. $\overline{WE}$ and $\overline{HSB}$ must be HIGH during SRAM Read cycles.
10. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both Low.
11. Measured ±200 mV from steady state output voltage.

[+] Feedback

SRAM Write Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{WC}	t_{AVAV}	Write Cycle Time	25		35		45		ns
t_{PWE}	t_{WLWH}, t_{WLEH}	Write Pulse Width	20		25		30		ns
t_{SCE}	t_{ELWH}, t_{ELEH}	Chip Enable To End of Write	20		25		30		ns
t_{SD}	t_{DVWH}, t_{DVEH}	Data Setup to End of Write	10		12		15		ns
t_{HD}	t_{WHDX}, t_{EHDX}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AVWH}, t_{AVEH}	Address Setup to End of Write	20		25		30		ns
t_{SA}	t_{AVWL}, t_{AVEL}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WHAX}, t_{EHAX}	Address Hold After End of Write	0		0		0		ns
t_{HZWE} [11,12]	t_{WLQZ}	Write Enable to Output Disable		10		13		15	ns
t_{LZWE} [11]	t_{WHQX}	Output Active After End of Write	5		5		5		ns

Switching Waveforms

Figure 9. SRAM Write Cycle 1: $\overline{WE}$ Controlled [13, 14]

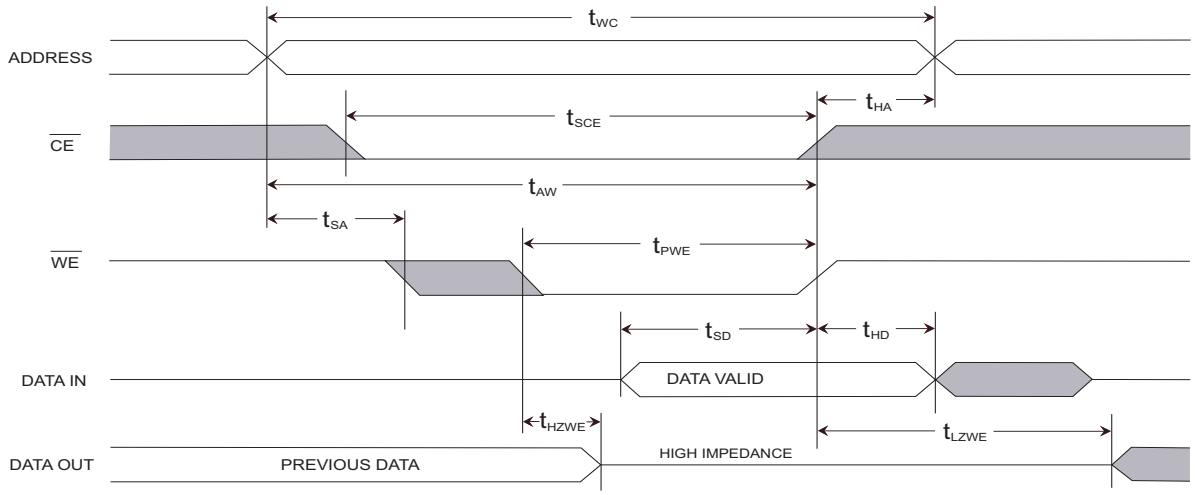
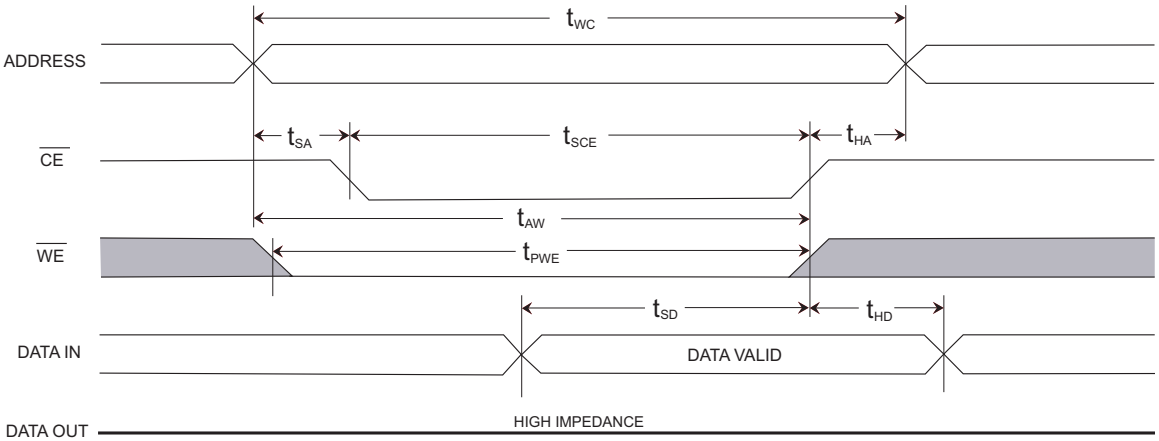


Figure 10. SRAM Write Cycle 2: $\overline{CE}$ Controlled [13, 14]



Notes
12. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
13. $\overline{HSB}$ must be high during SRAM WRITE cycles.
14. $\overline{CE}$ or $\overline{WE}$ must be greater than V_{IH} during address transitions.

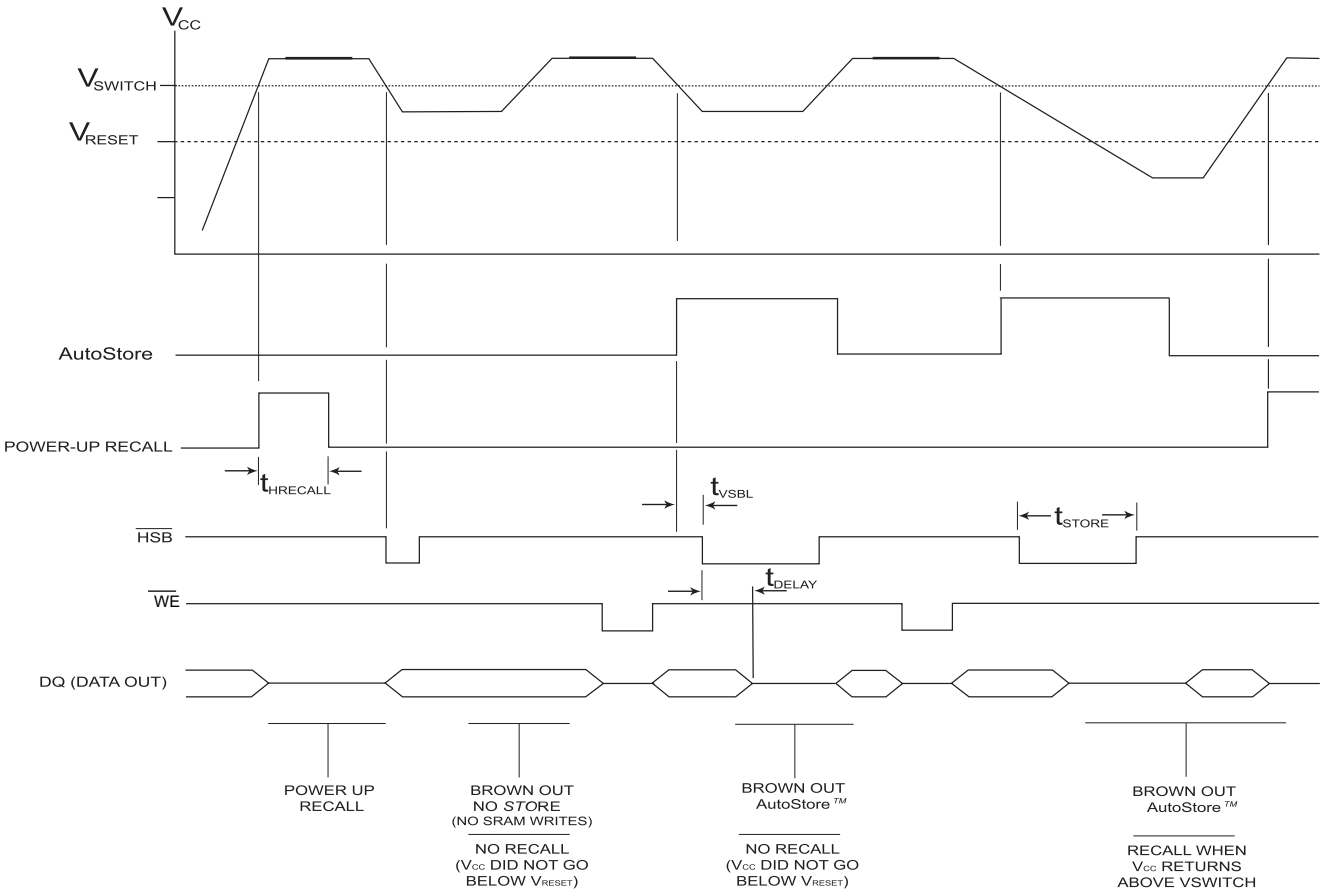
[+] Feedback

AutoStore or Power Up RECALL

Parameter	Alt	Description	CY14E256L		Unit
			Min	Max	
$t_{HRECALL}$ [15]	$t_{RESTORE}$	Power up RECALL Duration		550	µs
t_{STORE} [16]	t_{HLHZ}	STORE Cycle Duration		10	ms
t_{DELAY} [16]	t_{HLQZ} , t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs
V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V
V_{RESET}		Low Voltage Reset Level		3.6	V
$t_{VCCRISE}$		V_{CC} Rise Time	150		µs
t_{VSBL} [13]		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ low		300	ns

Switching Waveforms

Figure 11. AutoStore/Power Up RECALL



Notes

15. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
16. $\overline{CE}$ and $\overline{OE}$ low and $\overline{WE}$ high for output behavior.
17. $\overline{HSB}$ is asserted low for 1us when V_{CAP} drops through V_{SWITCH}. If an SRAM WRITE has not taken place since the last nonvolatile cycle, $\overline{HSB}$ is released and no store takes place.

[+] Feedback

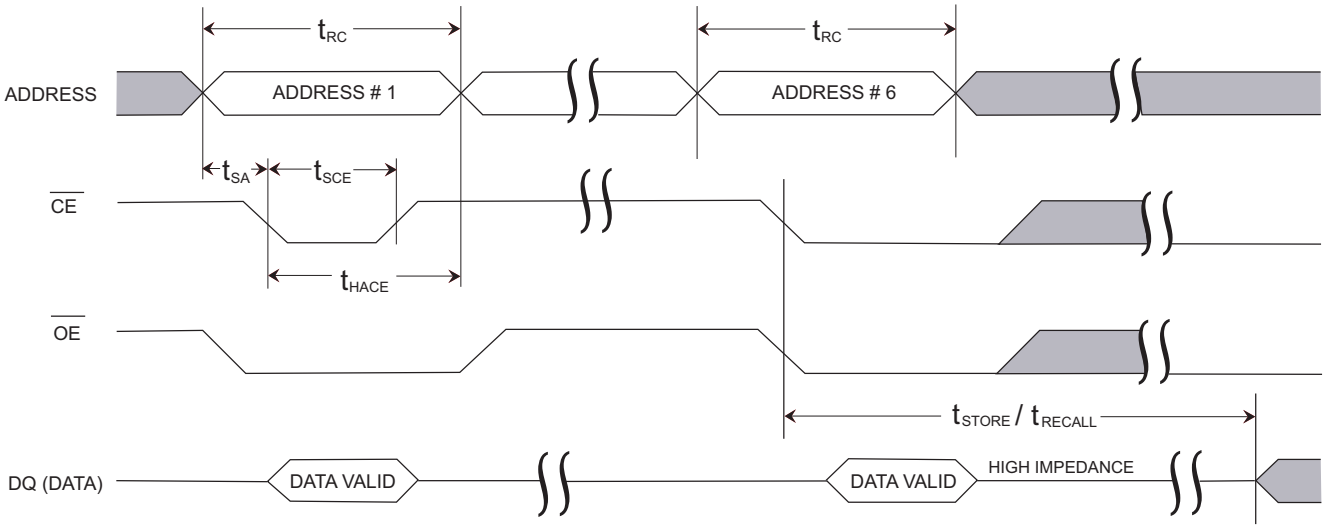
Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [19]

Parameter	Alt	Description	25 ns		35 ns		45 ns		Unit
			Min	Max	Min	Max	Min	Max	
t_{RC}[16]	t_{AVAV}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t_{SA}[18, 19]	t_{AVEL}	Address Setup Time	0		0		0		ns
t_{CW}[18, 19]	t_{ELEH}	Clock Pulse Width	20		25		30		ns
t_{HACE}[18, 19]	t_{ELAX}	Address Hold Time	20		20		20		ns
t_{RECALL}		RECALL Duration		20		20		20	µs

Switching Waveforms

Figure 12. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [19]



Notes
18. The software sequence is clocked on the falling edge of $\overline{CE}$ without involving $\overline{OE}$ (double clocking aborts the sequence).
19. The six consecutive addresses must be read in the order listed in the Mode Selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.

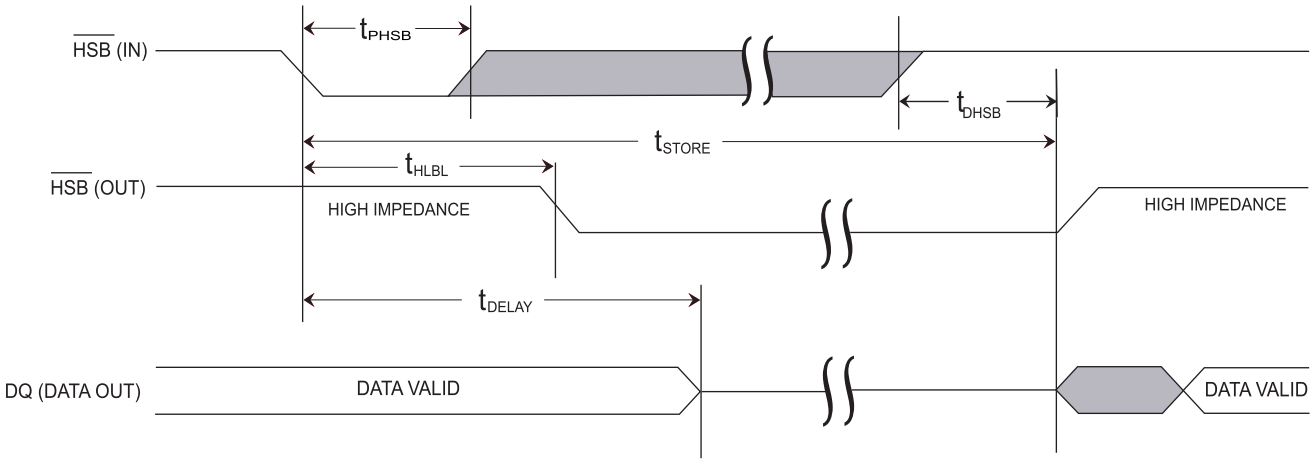
[+] Feedback

Hardware STORE Cycle

Parameter	Alt	Description	CY14E256L		Unit
			Min	Max	
t_{DHSB} [16, 20]	$t_{RECOVER}$, t_{HHQX}	Hardware STORE High to Inhibit Off		700	ns
t_{PHSB}	t_{HLHX}	Hardware STORE Pulse Width	15		ns
t_{HLBL}		Hardware STORE Low to STORE Busy		300	ns

Switching Waveforms

Figure 13. Hardware STORE Cycle

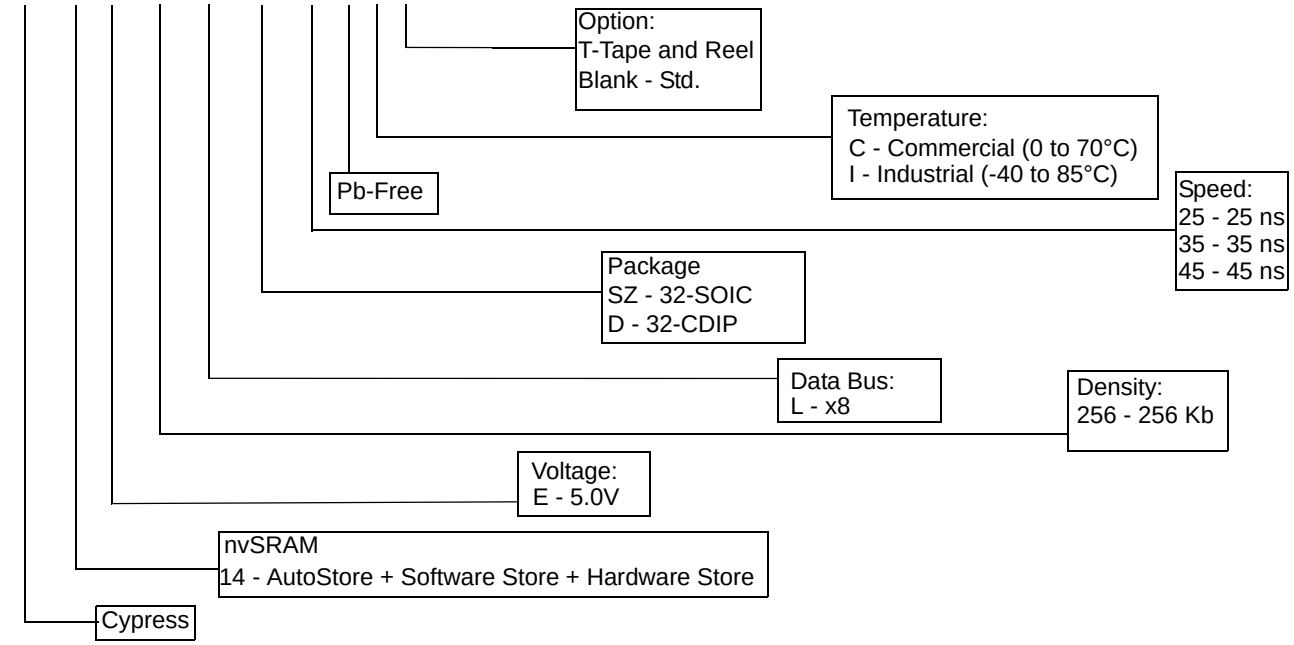


Note
20. t_{DHSB} is only applicable after t_{STORE} is complete.

[+] Feedback

Part Numbering Nomenclature (Commercial and Industrial)

CY 14 E 256 L- SZ 25 X C T



Ordering Information

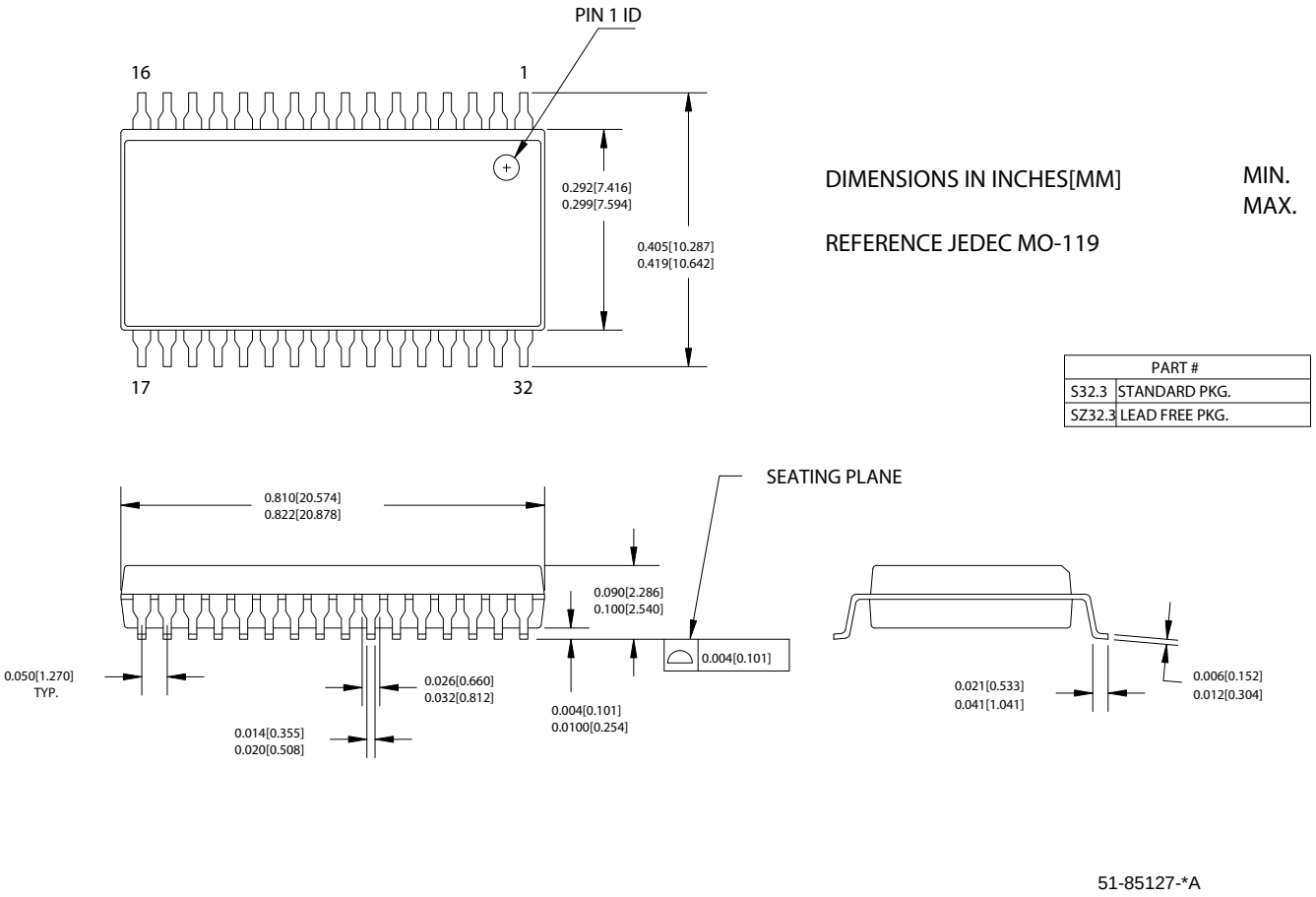
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14E256L-SZ25XCT	51-85127	32-pin SOIC (300 mil)	Commercial
	CY14E256L-SZ25XC	51-85127	32-pin SOIC (300 mil)	
	CY14E256L-SZ25XIT	51-85127	32-pin SOIC (300 mil)	Industrial
	CY14E256L-SZ25XI	51-85127	32-pin SOIC (300 mil)	
35	CY14E256L-SZ35XCT	51-85127	32-pin SOIC (300 mil)	Commercial
	CY14E256L-SZ35XC	51-85127	32-pin SOIC (300 mil)	
	CY14E256L-SZ35XIT	51-85127	32-pin SOIC (300 mil)	Industrial
	CY14E256L-SZ35XI	51-85127	32-pin SOIC (300 mil)	
45	CY14E256L-SZ45XCT	51-85127	32-pin SOIC (300 mil)	Commercial
	CY14E256L-SZ45XC	51-85127	32-pin SOIC (300 mil)	
	CY14E256L-SZ45XIT	51-85127	32-pin SOIC (300 mil)	Industrial
	CY14E256L-SZ45XI	51-85127	32-pin SOIC (300 mil)	
	CY14E256L-D45XI	001-51694	32-pin CDIP (300 mil)	

All parts are Pb-free. The above table contains Final information. Please contact your local Cypress sales representative for availability of these parts

[+] Feedback

Package Diagram

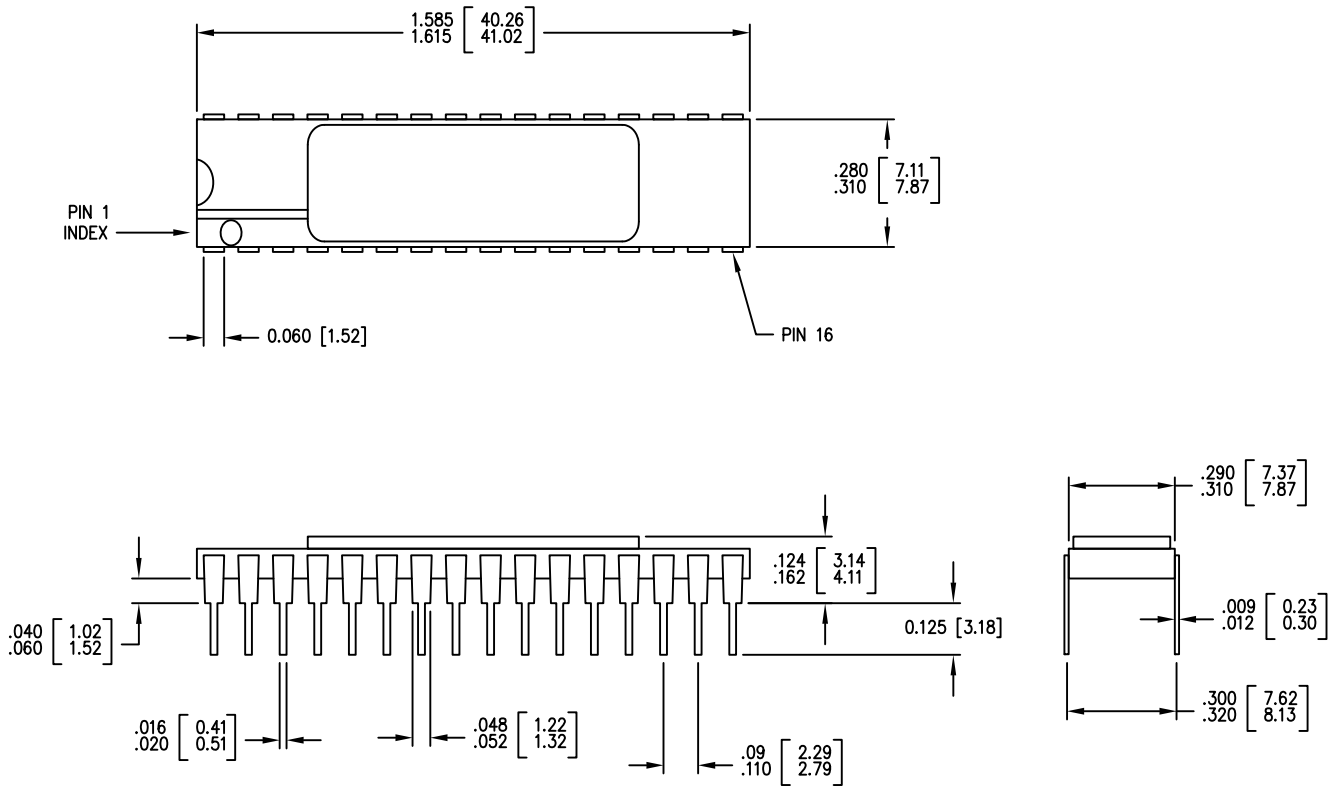
Figure 14. 32-Pin (300 Mil) SOIC (51-85127)



[+] Feedback

Package Diagram (continued)

Figure 15. 32-Pin (300 Mil) CDIP (001-51694)



1. ALL DIMENSIONS ARE IN MILLIMETERS AND INCHS [MIN/MAX]
2. PACKAGE WEIGHT : TBD

001-51694 **

[+] Feedback

Document History Page

Document Title: CY14E256L 256 Kbit (32K x 8) nvSRAM Document Number: 001-06968				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	427789	See ECN	TUP	New data sheet
*A	437321	See ECN	TUP	Show data sheet on external Web
*B	472053	See ECN	TUP	Updated Part Numbering Nomenclature and Ordering Information
*C	503290	See ECN	PCI	Changed from “Advance” to “Preliminary” Changed the term “Unlimited” to “Infinite” Changed I_{CC3} value from 10mA to 15mA Removed Industrial Grade mention Removed 35 ns speed bin Removed I_{CC1} values from the DC table for 35 ns Industrial Grade Corrected V_{IL} min specification from (V_{CC} - 0.5) to (V_{SS} - 0.5) Removed all references pertaining to $\overline{OE}$ controlled Software STORE and RECALL operation Changed the address locations of the software STORE/RECALL command Updated Part Nomenclature Table and Ordering Information Table
*D	1349963	See ECN	UHA/SFV	Changed from “Preliminary” to “Final.” Updated AC Test Conditions Updated Ordering Information Table
*E	2427986	See ECN	GVCH	Move to external web
*F	2606744	02/19/09	GVCH/PYRS	Updated Feature Section Added 35 ns access speed specs Added CDIP package Removed HSB ganging feature Added footnote 5 Updates all the notes Added Best practices Added Industrial specs Changed Icc3 from 15 mA to 10 mA Added I_{SB1} spec Added parameter V_{BL} Changed V_{IH} test conditions from -2 and 4 to -4 and 8mA Added footnote 6 and 7 Added t_{VSBL} and V_{RESET} parameter to Autostore or Power-up Recall table Added Thermal resistance values Changed parameter t_{AS} to t_{SA} Renamed t_{GLAX} to t_{HACE} Renamed $t_{RESTORE}$ to t_{DHSB} Updated Figure 13

[+] Feedback

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